Tutorial Proposal for PACT’2012

Title: Emerging Nonvolatile Memory Applications in Computer Architecture

Organizers:
Prof. Yiran Chen, yic52@pitt.edu
Electrical and Computer Engineering Department, University of Pittsburgh

Format: Three 55-min presentations with 15-min Q&A

Tutorial Description:
Emerging nonvolatile memory technologies offers tremendous opportunities to enhance the present-day computer architecture from various aspects, such as storage capacity, power, computing structure, system performance and robustness. In this tutorial, we invited three speakers to present their state-of-the-art research on the applications of three emerging memory technologies in the modern memory hierarchy designs, including spin-transfer torque random access memory (STT-RAM), phase change memory (PCM) and resistive RAM (RRAM). The complimentary backgrounds of our speakers provide a comprehensive review on the three promising emerging memory technologies across multiple layers from device and circuit design to architecture that is specifically emphasized in our tutorial.

Planned Talks:
Prof. Yiran Chen (confirmed)
Electrical and Computer Engineering Department, University of Pittsburgh
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Title: The Critical Issues in the Applications of STT-RAM in Modern Memory Hierarchy.

Abstract:
The continuously increased technical challenges for the scaling of mainstream memory technologies inspired the tremendous investment on the next-generation nonvolatile memory technologies. As one of the most promising candidates, spin-transfer torque random access memory (STT-RAM), which is inspired by the magnetic head technology in Hard Disk Drive, features many attractive characteristics such as non-volatility, high cell density, nanosecond access time and low operating voltage etc. This presentation will start with the general introduction on STT-RAM technology. After that, we will discuss some interesting properties of STT-RAM designs, including the reliability and asymmetry of read and write operations, the data-pattern dependent writability, the tradeoff between non-volatility and memory robustness, and the scaling trend etc. Some spin-based circuit designs, applications, and statistical STT-RAM models for architecture-level research will be also presented at the end of our talk. We hope the presentation can offer the audiences a comprehensive review on the basics of STT-RAM and the relevant state-of-the-art research.

Biography:
Yiran Chen received B.S. and M.S. (both with honors) in EE from Tsinghua University, China and Ph.D. in ECE from Purdue University, W. Lafayette, IN. Before he joined University of Pittsburgh in 2010, he worked with Synopsys and Seagate for 5 years. Dr. Chen’s research interests include VLSI design, nano-electronic devices and embedded systems. He has published more than 90 technical publications, has 53 granted US patents and other 23 pending applications. He coauthored one book – “Nonvolatile Memory Design: Magnetic, Resistive, and Phase Changing”, as well as other several book chapters. He is the associate editor of TCAD and the editor of JCIT. He served as technical and organizational committees of many conferences, including DAC, ICCAD, DATE, ASP-DAC, ISLPED,
FPT, ISCAS, CODES+ISSS, etc. During 2007-2010, he served as the patent review board member of Seagate memory product group. As a key developer of PrimeTimeVX, Dr. Chen received "The hot 100 products of 2006" from EDN, “EDN 100 Hot Products Distinction” from Synopsys and the finalist of "Prestigious 2007 DesignVision Awards" from IEC. His works also received two best paper awards from ISQED 2008 and ISLPED 2010, respectively, and were nominated as the best paper candidates in ISQED, DATE, and ASPDAC etc. for multiple times. His Ph.D. student is the recipient of A. Richard Newton Scholarship. He is the inventor of “Spintronic Memristor”.

Prof. Youtao Zhang (confirmed)
Computer Science Department, University of Pittsburgh
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Title: Addressing Power and Latency Challenges of Multi-level Cell Phase Change Memory

Abstract:
Phase change memory (PCM) recently has emerged as a promising technology to meet the fast growing demand for large capacity memory in modern computer systems. In particular, multi-level cell (MLC) PCM that stores multiple bits in a single cell, offers high density with low per-byte fabrication cost. However, integrating MLC PCM into existing memory hierarchy faces severe power and latency challenges.

In this tutorial, we will discuss how MLC PCM works and survey existing works in MLC PCM. In particular, we will elaborate the use of error correction code (ECC) to mitigate non-negligible process variation in MLC PCM chips. Our experimental results show that adopting ECC helps to significantly reduce RESET power, improve MLC PCM write latency, and prolong the lifetime of MLC PCM chips.

Biography:
Youtao Zhang received the PhD degree in computer science from the University of Arizona in 2002. He is an associate professor in Computer Science Department, University Pittsburgh. His research interests are in the areas of computer architecture, program analysis and optimization. He is the recipient of US NSF CAREER Award in 2005, the distinguished paper award of the IEEE/ACM International Conference on Software Engineering (ICSE) conference in 2003, the most original paper award of the International Conference on Parallel Processing (ICPP) conference in 2003. He is a member of the ACM and the IEEE.

Prof. Guangyu Sun (confirmed)
Center for Energy Efficient Computing and Applications (CECA), Peking University
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Title: Circuit and architecture level design exploration of RRAM

Abstract:
The emerging memristor-based Resistive RAM (ReRAM) has shown attractive properties, such as high density, low-power, good-scalability, and non-volatility. These properties make ReRAM one of most promising memory technologies for future memory hierarchy design. The efficient adoption of ReRAM in memory hierarchy, however, requires improvement in both circuit and architecture levels. In the circuit level, we propose a dual-element memory structure to satisfy design constraints which are usually difficult to be satisfied with one-cell memory structure. In addition, we study and characterize the impact of process variations on the electrical behaviors of the memristor and its implication to the circuit design. In order to mitigate the impact of process variations, we improve ECC code to relax the Bit Error Rate (BER) requirement of ReRAM based on the mathematical analysis of error patterns. With the help of circuit and architecture level techniques, the trade-off among the energy, speed, and distinguishability is explored for different design objectives. In particular, we show that our techniques can help improve
energy efficiency of ReRAM without violating design constraints, such as programming speed and distinguishability.

Biography

Dr. Guangyu Sun is an assistant professor in the Center for Energy Efficient Computing and Applications (CECA) at the Peking University. He received his BS and MS degrees from the Tsinghua University and received his Ph.D. degree in Computer Engineering from the Pennsylvania State University. Dr. Guangyu Sun’s research interests are in the field of computer architecture with an emphasis on memory systems and three dimension (3D) architectures. He is also interested in heterogeneous processor architecture, 3D, and process-variation aware VLSI design. Recently, he has extensively researched on the design exploration of different emerging memory technologies, such as STTRAM and ReRAM, in architecture and circuit levels. Dr. Guangyu Sun has published about 30 papers in different research fields. For the research of emerging memory technologies, he has published about 15 refereed papers in both architecture and EDA conferences including ISCA, HPCA, DAC, etc. His work introduced circuit and architectural levels of modeling of different emerging memory technologies. He also presented a holistic study of using various emerging memory technologies in different levels of memory hierarchy, ranging from on-chip cache to SSD. He has proposed several novel architectures, such as hybrid cache/SSD, to facilitate the adoption of these memories.